Claims:

1. A method of measuring a DUT comprising the steps of:

   providing a vector network analyzer having at least two measurement ports,

   measuring a reflection characteristic of a high reflect calibration standard at each measurement port,

   measuring forward and reverse reflection and transmission characteristics of a line calibration standard,

   measuring forward and reverse reflection and transmission characteristics of a source terminated through calibration standard,

   measuring forward and reverse reflection and transmission characteristics of a locally terminated through calibration standard,

   calculating error coefficients for said at least two measurement ports based upon results in said steps of measuring,

   calculating a shifted electrical length attributable to said calibration standards based upon results in said steps of measuring,

   measuring a DUT,

   correcting for systematic errors in said step of measuring said DUT based upon said error coefficients to yield a corrected S-parameter

matrix, and

shifting a reference plane for each element of said
corrected S-parameter matrix to coincide with a
DUT measurement plane.

2. A method of measuring as recited in claim 1 wherein
said vector network analyzer comprises more than two
measurement ports and wherein said steps of
measuring are repeated for all direct pairs of said
measurement ports and further comprising the step of
measuring a locally terminated through calibration
standard for all indirect pairs of measurement
ports.

3. A method of measuring as recited in claim 2 wherein
a shifted electrical length between said indirect
pairs is calculated using load match and source
match error coefficient terms.

4. A method of measuring as recited in claim 3 wherein

$$\frac{\Gamma_{SA\_portn}}{\Gamma_{LA\_portm}} = S_{21\_thru\_nm}S_{12\_thru\_nm}$$

wherein $S_{21\_thru\_nm}$ is equal to $S_{12\_thru\_mn}$ and an argument
of both solutions for $S_{21\_thru\_nm}$ is fit to a straight
line, the solution having a y-intercept closest to zero
being the correct solution and the resulting argument
of the correct solution being the electrical delay.

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5. A method of measuring as recited in claim 2 and further comprising the step of measuring forward and reverse reflection and transmission characteristics of a source terminated through calibration standard for indirect pairs of said measurement ports.

6. A method of measuring as recited in claim 2 wherein transmission tracking error coefficients are calculated using an averaging process for all proximal pairs.

7. A method of measuring as recited in claim 5 wherein said step of calculating further comprises calculating a different respective shifted electrical length for each said direct and indirect pair.

8. A method of measuring as recited in claim 7 wherein said shifted electrical length between proximal pairs is determined by averaging a shifted electrical length between said direct pair and said indirect pair having respective proximal pair measurement ports in common.

9. A method of measuring as recited in claim 5 and further comprising the step of measuring forward and reverse reflection and transmission characteristics

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of a locally terminated through calibration standard for proximal pairs of said measurement ports.

10.   A method of measuring as recited in claim 9 wherein transmission tracking error coefficients are calculated using said locally terminated through calibration standard for said proximal pairs.

11.   A method of measuring as recited in claim 2 wherein said vector network analyzer comprises a multiport test set and switch matrix having said more than two measurement ports.

12.   A method of measuring as recited in claim 1 and further comprising the step of determining a type of high reflect calibration standard.

13.   A method of measuring as recited in claim 12 wherein said step of determining further comprises calculating a characteristic of said high reflect calibration standard, fitting arguments of two possible solutions for said characteristics to a straight line, identifying which solution is closest to zero phase at DC.

14.   A method of measuring as recited in claim 1 wherein said ten error coefficients comprise forward

and reverse reflection tracking error coefficients,
wherein said forward and reverse reflection tracking
error coefficients are determined using a boundary
condition wherein an argument of reflection tracking
is zero at DC.

15.   A method of measuring as recited in claim 7 and
wherein said step of shifting comprises modifying an
argument of respective S-parameters of said measured
DUT according to respective ones of said shifted
electrical lengths.

16.   A method of measuring as recited in claim 15
wherein said step of shifting a reference plane
comprises adjusting each said element of said
corrected S-parameter matrix according to:

$$S_{dut} = \mid \rho \mid e^{-j(\theta_0 + \delta\theta(f))}$$

wherein δθ is calculated from said electrical length
as a function of frequency.

17.   A method of measuring as recited in claim 1
wherein said step of calculating a shifted
electrical length comprises calculating a
characteristic of said high reflect calibration
standard, fitting an argument of said characteristic
to a straight line, and using a slope of said
straight line to calculate a shifted electrical
length.

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18.   A method of measuring comprising the steps of:

providing a vector network analyzer having at least two measurement ports,

measuring a reflection characteristic of a high reflect calibration standard for each said measurement port,

measuring forward and reverse reflection and transmission characteristics of a line calibration standard between said at least two measurement ports,

measuring forward and reverse reflection and transmission characteristics of a source terminated through between said at least two measurement ports,

measuring forward and reverse reflection and transmission characteristics of a locally terminated through calibration standard between said at least two measurement ports,

calculating forward and reverse reflection tracking error coefficients based upon results from said steps of measuring using a boundary condition wherein an argument of said reflection tracking coefficients are zero at DC,

calculating all remaining forward and reverse error coefficients,

measuring a DUT,

correcting for systematic errors in said step of

measuring said DUT based upon said error

coefficients.

19.   A method of measuring as recited in claim 18

wherein said vector network analyzer comprises more

than two measurement ports and wherein said steps of

measuring are repeated for direct pairs of said

measurement ports and further comprising the step of

measuring a locally terminated through calibration

standard between indirect pairs of said measurement

ports.

20.   A method of measuring as recited in claim 18

and further comprising the steps of calculating an

electrical length of a shifted reference plane for

each said at least two measurement ports based upon

results in said steps of measuring and correcting

said shifted reference plane to coincide with a DUT

measurement plane.

21.   A method of measuring as recited in claim 20

wherein said step of calculating a shifted

electrical length comprises calculating a

characteristic of a high reflect calibration

standard, fitting an argument of said characteristic

to a straight line and using a slope of said

straight line to calculate a shifted electrical

length.

22.   A method of measuring as recited in claim 19
wherein said steps of measuring a DUT and correcting
for systematic errors yields a corrected S-parameter
matrix and further comprising the steps of
calculating a respective electrical length of a
shifted reference plane for each direct pair of
measurement ports based upon results in said steps
of measuring and shifting respective elements of
said corrected S-parameter matrix by respective
electrical lengths to coincide with a DUT
measurement plane.

23.   A method of measuring as recited in claim 20
wherein said step of shifting said shifted reference
plane comprises adjusting each said element of said
corrected S-parameter matrix according to:

$$S_{dut} = |\rho| e^{-j(\theta_0 + \delta\theta(f))}$$

wherein δ(θ) is calculated from said electrical length
as a function of frequency.

24.   A method of measuring as recited in claim 18
and further comprising the step of determining
whether said high reflect calibration standard is an
open circuit or a short circuit.

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25.   A method of measuring as recited in claim 24
wherein said step of determining further comprises
fitting arguments of two possible solutions for a
reflection tracking error coefficient to a straight
line and identifying which solution is closest to
zero phase at DC.

26.   A method of measuring as recited in claim 19
wherein a shifted electrical length between said
indirect pairs is calculated using load match and
source match error coefficient terms.

27.   A method of measuring as recited in claim 26
wherein

$$\frac{\Gamma_{SA\_portn}}{\Gamma_{LA\_portm}} = S_{21\_thru\_nm} S_{12\_thru\_nm}$$

and $S_{21\_thru\_nm}$ is equal to $S_{12\_thru\_mn}$ and an argument of
both solutions for $S_{21\_thru\_nm}$ is fit to a straight line,
the solution having a y-intercept closest to zero being
the correct solution and the resulting argument of the
correct solution being used to determine said shifted
electrical length.

28.   A method of measuring as recited in claim 19
and further comprising the step of measuring forward
and reverse reflection and transmission
characteristics of a source terminated through
calibration standard for indirect pairs of said

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measurement ports.

29.   A method of measuring as recited in claim 28
and further comprising calculating a shifted
electrical length for each direct and indirect pair
of measurement ports.

30.   A method of measuring as recited in claim 29
wherein transmission tracking error coefficients are
calculated using an averaging process for all
proximal pairs of measurement ports.

31.   A method of measuring as recited in claim 28
wherein said shifted electrical length between
proximal pairs is determined by averaging a shifted
electrical length between said direct pair and said
indirect pair having respective proximal pair
measurement ports in common.

32.   A method of measuring as recited in claim 28
and further comprising the step of measuring forward
and reverse reflection and transmission
characteristics of a locally terminated through
calibration standard for proximal pairs of said
measurement ports.

33.   A method of measuring as recited in claim 32

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wherein transmission tracking error coefficients are
calculated using results of measurement taken of
said locally terminated through calibration standard
for said proximal pairs.

34.   An apparatus for measuring a DUT comprising:

a vector network analyzer comprising a signal
        generator and at least two receivers capable of
        connection to at least two measurement ports,

means for measuring a reflection characteristic of a
        high reflect calibration standard at each
        measurement port, measuring forward and reverse
        reflection and transmission characteristics of
        a line calibration standard, measuring forward
        and reverse reflection and transmission
        characteristics of a source terminated through
        calibration standard, measuring forward and
        reverse reflection and transmission
        characteristics of a locally terminated through
        calibration standard,

means for calculating ten error coefficients for
        said at least two measurement ports based upon
        results of said means for measuring,

means for measuring the DUT,

a processor for calculating a shifted electrical
        length attributable to said calibration
        standards, for correcting systematic errors in
        results from said means for measuring said DUT

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based upon said error coefficients to yield a
corrected S-parameter matrix, and for shifting
a reference plane for each element of said
corrected S-parameter matrix to coincide with a
DUT measurement plane.

35.   An apparatus as recited in claim 34 wherein
said vector network analyzer comprises more than two
measurement ports and wherein said means for
measuring further comprises means for measuring a
locally terminated through calibration standard for
indirect pairs of measurement ports.

36.   An apparatus as recited in claim 35 wherein
said processor calculates a respective shifted
electrical length between said indirect pairs using
load match and source match error coefficient terms.

37.   An apparatus as recited in claim 36 wherein

$$\frac{\Gamma_{SA\_portn}}{\Gamma_{LA\_portm}} = S_{21\_thru\_nm}S_{12\_thru\_nm}$$

and $S_{21\_thru\_nm}$ is equal to $S_{12\_thru\_mn}$ and an argument of
both solutions for $S_{21\_thru\_nm}$ is fit to a straight line,
the solution having a y-intercept closest to zero being
a correct solution and a resulting argument of said
correct solution being used to determine said shifted
electrical delay.

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38.   An apparatus as recited in claim 35 wherein
said processor calculates transmission tracking
error coefficients for said proximal pairs using an
averaging process.

39.   An apparatus as recited in claim 35 and further
comprising means for measuring forward and reverse
reflection and transmission characteristics of a
source terminated through calibration standard
between indirect pairs of measurement ports.

40.   An apparatus as recited in claim 39 wherein
said processor calculates different respective
shifted electrical lengths for said direct and
indirect pairs of measurement ports.

41.   An apparatus as recited in claim 40 wherein
said processor calculates said shifted electrical
length between proximal pairs by averaging a shifted
electrical length between said direct pair and said
indirect pair having respective proximal pair
measurement ports in common.

42.   An apparatus as recited in claim 39 wherein
said means for measuring further comprising means
for measuring forward and reverse reflection and
transmission characteristics of a locally terminated
through calibration standard for proximal pairs of

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said measurement ports.

43.   An apparatus as recited in claim 42 wherein said processor calculates transmission tracking error coefficients using results from said means for measuring said locally terminated through calibration standard for said proximal pairs.

44.   An apparatus as recited in claim 35 and further comprising a multiport test set and switch matrix connected to said vector network analyzer for providing more than two of said measurement ports.

45.   An apparatus as recited in claim 34 and further comprising means for determining a type of said high reflect calibration standard.

46.   An apparatus as recited in claim 45 wherein said means for determining further comprises means for fitting arguments of two possible solutions for a reflection tracking error coefficient to a straight line and means for identifying which solution is closest to zero phase at DC.

47.   An apparatus as recited in claim 34 wherein said ten error coefficients comprise forward and reverse reflection tracking error coefficients and

said means for calculating determines said forward
and reverse reflection tracking error coefficients
using a boundary condition wherein an argument of
reflection tracking is zero at DC.

48.   An apparatus as recited in claim 34 wherein
said measurement ports comprise direct pairs of
measurement ports and indirect pairs of measurement
ports and wherein said means for calculating said
shifted electrical length comprises means for
calculating respective ones of said shifted
electrical lengths for each direct and indirect pair
of measurement ports.

49.   An apparatus as recited in claim 48 and wherein
said processor for shifting modifies an argument of
respective S-parameters of said measured DUT
according to respective ones of said shifted
electrical lengths.

50.   An apparatus as recited in claim 49 wherein
said processor for shifting modifies respective
elements of said corrected S-parameter matrix
according to:

$$S_{dut} = |\rho| e^{-j(\theta_0 + \delta\theta(f))}$$

wherein δθ is calculated from said electrical length as
a function of frequency.

51.   An apparatus as recited in claim 48 wherein
said processor calculates said shifted electrical
length by fitting an argument of a characteristic of
a high reflect calibration standard to a straight
line and using a slope of said straight line to
calculate a shifted electrical length.

52.   An apparatus for measuring comprises:

a vector network analyzer having at least two
        measurement ports,

means for measuring a reflection characteristic for
        each said measurement port, measuring forward
        and reverse reflection and transmission
        characteristics for a line calibration standard
        between said at least two measurement ports
        and, measuring forward and reverse reflection
        and transmission characteristics of a source
        terminated through calibration standard between
        said at least two measurement ports, and
        measuring forward and reverse reflection and
        transmission characteristics of a locally
        terminated through calibration standard between
        said at least two measurement ports,

a processor for calculating forward and reverse
        reflection tracking error coefficients based
        upon a boundary condition wherein an argument
        of said reflection tracking error coefficients
        is zero at DC, and for calculating all
        remaining forward and reverse error

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coefficients,

means for measuring a DUT,

said processor correcting for systematic errors in
said means for measuring said DUT based upon
said error coefficients.

53.   An apparatus as recited in claim 52 wherein
said vector network analyzer comprises more than two
measurement ports and wherein said means for
measuring measures all direct pairs of said
measurement ports and further comprising means for
measuring forward and reverse reflection and
transmission characteristics of a locally terminated
through calibration standard between indirect pairs
of measurement ports.

54.   An apparatus as recited in claim 52 wherein
said processor calculates an electrical length of a
shifted reference plane for each said at least two
measurement ports and corrects said shifted
reference plane to coincide with a DUT measurement
plane.

55.   An apparatus as recited in claim 53 wherein
said processor calculates respective electrical
lengths of a shifted reference plane for each said
direct pair of measurement ports and corrects said
shifted reference plane for each said direct pair to

coincide with a DUT measurement plane.

56.   An apparatus as recited in claim 55 wherein
said processor calculates said shifted electrical
lengths by fitting an argument of a characteristic
of a high reflect calibration standard to a straight
line and using a slope of said straight line to
calculate said shifted electrical length.

57.   An apparatus as recited in claim 55 wherein
said processor shifts said shifted reference plane
by adjusting respective elements of a corrected S-
parameter matrix according to:

$$S_{dut} = |\rho| e^{-j(\theta_0 + \delta\theta(f))}$$

wherein $\delta\theta$ is calculated from said respective
electrical length as a function of frequency.

58.   An apparatus as recited in claim 52, said
processor also determining a type of said high
reflect calibration standard.

59.   An apparatus as recited in claim 58 wherein
said processor determines said type of high reflect
standard by fitting arguments of two possible
solutions for a reflection tracking error
coefficient to a straight line and identifying which
solution is closest to zero phase at DC.

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60.   An apparatus as recited in claim 53 wherein
said processor calculates a shifted electrical
length between said indirect pairs using load match
and source match error coefficient terms.

61.   An apparatus as recited in claim 60 wherein

$$\frac{\Gamma_{SA\_portn}}{\Gamma_{LA\_portm}} = S_{21\_thru\_nm} S_{12\_thru\_nm}$$

and $S_{21\_thru\_nm}$ is equal to $S_{12\_thru\_mn}$ and an argument of
both solutions for $S_{21\_thru\_nm}$ is fit to a straight line,
the solution having a y-intercept closest to zero being
the correct solution and the resulting argument of the
correct solution being the electrical delay.

62.   An apparatus as recited in claim 54 and further
comprising means for measuring forward and reverse
reflection and transmission characteristics of a
source terminated through calibration standard
between indirect pairs of measurement ports.

63.   An apparatus as recited in claim 62 wherein
said processor calculates a different respective
shifted electrical length between each direct and
indirect pair of measurement ports.

64.   An apparatus as recited in claim 63 and wherein

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said processor for shifting modifies an argument of respective S-parameters of said measured DUT according to respective ones of said shifted electrical lengths.

65.   An apparatus as recited in claim 64 wherein said processor shifts said shifted reference plane by adjusting respective elements of a corrected S-parameter matrix according to:

$$S_{dutl} = |\rho| e^{-j(\theta_0 + \delta\theta(f))}$$

wherein δθ is calculated from said respective electrical length as a function of frequency.

66.   An apparatus as recited in claim 63 wherein said processor calculates a shifted electrical length between proximal pairs by averaging a shifted electrical length between said direct pair and said indirect pair having respective proximal pair measurement ports in common.

67.   An apparatus as recited in claim 63 wherein said means for measuring further comprises means for measuring forward and reverse reflection and transmission characteristics of a locally terminated through calibration standard for proximal pairs of said measurement ports.

68. An apparatus as recited in claim 67 wherein said processor calculates transmission tracking error coefficients using results of a measurement of said locally terminated through calibration standard for said proximal pairs.

69. An apparatus as recited in claim 63 wherein said processor calculates a shifted electrical length for proximal pairs of measurement ports from an average of shifted electrical lengths for direct and indirect pairs having proximal pair measurement ports in common.

70. An apparatus as recited in claim 69 and wherein said processor for shifting modifies an argument of respective S-parameters of said measured DUT according to respective ones of said shifted electrical lengths.

71. A method of measuring a device under test comprising the steps of:

obtaining measured S-parameter characteristics of a reflect, a line, and a through calibration standard over a range of stimulus frequencies for each port of the device under test,

calculating forward and reverse reflection tracking error coefficients based upon results from said measured characteristics using a boundary

condition wherein an argument of said

reflection tracking coefficients are zero at

DC,

calculating all remaining forward and reverse error
coefficients,

obtaining measured S-parameters characteristics of a
DUT over said range of frequencies,

correcting for systematic errors in said measured S-
parameter characteristics of said DUT based
upon said error coefficients.

72.   Computer readable media tangibly embodying a
program of instructions executable by a computer to
perform a method of determining actual S-parameter
characteristics of a device under test based upon
measured S-parameter characteristics of said device
under test, the method comprising:
obtaining measured S-parameter characteristics of a
reflect, line, and through calibration
standards over a range of stimulus frequencies
for each port of the device under test,

calculating forward and reverse reflection tracking
error coefficients based upon results from said
measured characteristics using a boundary
condition wherein an argument of said
reflection tracking coefficients are zero at
DC,

calculating all remaining forward and reverse error
coefficients,

obtaining measured S-parameters characteristics of
said device under test over said range of
frequencies,

correcting for systematic errors in said measured S-
parameter characteristics of said device under
test based upon said error coefficients.